

IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity. Please enter these claims as amended. Also attached is a version with markings to show changes made to the claims.

- Amended*
1. (Amended three times) A metallization structure for a semiconductor device, comprising:
a substrate comprising a substantially planar upper surface; and
a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising:
a metal layer defining a pattern on a portion of the substrate upper surface;
a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls and said single conducting layer including an upper surface out of contact with any metal; and
metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer.
2. (Reiterated) The metallization structure of claim 1, further comprising a dielectric layer on the substrate upper surface and underlying the metal layer.
3. (Reiterated) The metallization structure of claim 2, wherein the dielectric layer is silicon oxide or BPSG.
4. (Reiterated) The metallization structure of claim 1, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

5. (Reiterated) The metallization structure of claim 4, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.
6. (Reiterated) The metallization structure of claim 5, wherein the first metal layer comprises titanium or titanium nitride.
7. (Reiterated) The metallization structure of claim 1, wherein the metal layer is titanium or titanium nitride.
8. (Previously amended) The metallization structure of claim 1, wherein the single conducting layer is selected from the group comprising aluminum and copper.
9. (Previously amended) The metallization structure of claim 8, wherein the single conducting layer is an aluminum-copper alloy.
10. (Reiterated) The metallization structure of claim 1, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.
11. (Previously twice amended) The metallization structure of claim 1, wherein the metal spacers are titanium or titanium nitride.
12. (Previously twice amended) The metallization structure of claim 1, further comprising a dielectric layer on the conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

13. (Reiterated) The metallization structure of claim 12, wherein the dielectric layer comprises a low dielectric constant material.

14. (Reiterated) The metallization structure of claim 13, wherein the dielectric layer is fluorine-doped silicon oxide.

15. (Reiterated) The metallization structure of claim 1, wherein the metal layer and the metal spacers comprise the same metal.

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16. (Amended three times) A metallization structure for a semiconductor device, comprising:
a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate;
a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture defining said conductive line;
a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture, said metal spacer in contact with said underlying metal layer; and
a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.

17. (Reiterated) The metallization structure of claim 16, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

18. (Reiterated) The metallization structure of claim 17, wherein the metal layer is titanium or titanium nitride.

19. (Previously amended) The metallization structure of claim 16, wherein the metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

20. (Previously amended) The metallization structure of claim 19, wherein the metal spacer is titanium or titanium nitride.

21. (Reiterated) The metallization structure of claim 16, wherein the substrate comprises a dielectric layer underlying the metal layer.

22. (Reiterated) The metallization structure of claim 21, wherein the dielectric layer underlying the metal layer is silicon oxide or BPSG.

23. (Amended twice) The metallization structure of claim 16, wherein the metal layer and the metal spacer comprise the same metal.

24. (Reiterated) The metallization structure of claim 16, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

25. (Reiterated) The metallization structure of claim 24, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

26. (Reiterated) The metallization structure of claim 16, further comprising at least one upper metal layer on the conductive layer and comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

27. (Reiterated) The metallization structure of claim 26, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

28. (Previously amended) The metallization structure of claim 26, wherein the at least one upper metal layer comprises titanium or titanium nitride.

100. (Reiterated) The metallization structure of claim 2, wherein said dielectric layer extends completely underneath said conductive line.

101. (Reiterated) The metallization structure of claim 16, wherein said aperture contains conductive material.

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102. (Amended twice) A structure for transmitting a signal across a semiconductor device, said structure comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line extending over said upper surface and isolated therefrom by a dielectric layer at least underlying said conductive line, said conductive line comprising:

a metal layer above said dielectric layer, said metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls, wherein an upper surface of said single conductive layer is out of contact with any metal; and

metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer

103. (Reiterated) The structure of claim 102, wherein the dielectric layer is silicon oxide or BPSG.

104. (Reiterated) The structure of claim 102, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

105. (Reiterated) The structure of claim 104, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

106. (Reiterated) The structure of claim 105, wherein the first metal layer comprises titanium or titanium nitride.

107. (Reiterated) The structure of claim 102, wherein the metal layer is titanium or titanium nitride.

108. (Previously amended) The structure of claim 102, wherein the single conducting layer is selected from the group comprising aluminum and copper.

109. (Previously amended) The structure of claim 108, wherein the single conducting layer is an aluminum-copper alloy.

110. (Reiterated) The structure of claim 102, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

111. (Reiterated) The structure of claim 102, wherein the metal spacers are titanium or titanium nitride.

112. (Previously amended) The structure of claim 102, further comprising a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

113. (Reiterated) The structure of claim 112, wherein the dielectric layer comprises a low dielectric constant material.

114. (Reiterated) The structure of claim 113, wherein the dielectric layer is fluorine-doped silicon oxide.

115. (Reiterated) The structure of claim 102, wherein the metal layer and the metal spacers comprise the same metal.

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116. (Amended twice) A structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising:
a substrate having a metal layer of a conductive line disposed thereon;
a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line;
a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture, said metal spacer in contact with said underlying metal layer; and
a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.

117. (Reiterated) The structure of claim 116, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

118. (Reiterated) The structure of claim 117, wherein the metal layer is titanium or titanium nitride.

119. (Reiterated) The structure of claim 116, wherein the metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

120. (Reiterated) The structure of claim 119, wherein the metal spacer is titanium or titanium nitride.

121. (Reiterated) The structure of claim 116, wherein the substrate comprises a dielectric layer underlying the metal layer.

122. (Reiterated) The structure of claim 121, wherein the dielectric layer underlying the metal layer is silicon oxide or BPSG.

123. (Reiterated) The structure of claim 116, wherein the metal layer and the metal spacer comprise the same metal.

124. (Reiterated) The structure of claim 116, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

125. (Reiterated) The structure of claim 124, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

126. (Reiterated) The structure of claim 116, further comprising at least one upper metal layer on the conductive layer and comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

127. (Reiterated) The structure of claim 126, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

128. (Reiterated) The structure of claim 126, wherein the at least one upper metal layer comprises titanium or titanium nitride.

129. (Reiterated) The structure of claim 116, wherein said metal spacer extends substantially a height of said at least one sidewall.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent 6,074,943 to Brennan et al.

Claims 1, 4 through 8, 10 through 13, and 15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Brennan et al. (U.S. Patent 6,074,943). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Brennan discloses a method of forming via structures using sidewalls as guides. Thus, as shown in FIG. 2H, Brennan discloses an Al-Cu layer 210 overlying an oxide layer 200 and an optional TiN barrier layer 205. A layer of anti-reflective coating (TiN) 215 is deposited on the Al-Cu layer 210. While Brennan teaches that the TiN barrier layer 205 is optional, it does not state that the anti-reflective coating 215 is optional. (Brennan, col. 2, lines 37-42). A layer of sidewall material 240 is deposited (FIG. 2E) and etched to an etch stop layer 220. The etch stop layer 220 is removed and a dielectric material 250 is deposited over the structure and sidewalls. (FIG. 2G). Brennan teaches that after the dielectric material 250 deposition is complete, “the sidewall material 240 will jut up into the ILD 250, forming sidewall extensions 260”. (Brennan, col. 2, lines 64-66). Subsequently, vias 270 are etched in the ILD layer 250 to contact the underlying interconnect. (FIG. 2H).

By way of contrast with Brennan, claim 1 as amended recites a metallization structure for a semiconductor device, comprising a substrate comprising a substantially planar upper surface; and a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising: a metal layer defining a pattern on a portion of the substrate upper surface; a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls and said single conducting layer

including an upper surface out of contact with any metal; and metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer.

Applicant respectfully submits that Brennan fails to disclose, either inherently or expressly, a conductive line comprising a metal layer defining a pattern on a portion of the substrate upper surface a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls and said single conducting layer including an upper surface out of contact with any metal and metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer. Instead, Brennan teaches that barrier layer 205 is optional. (Brennan, col.2, lines 37-38).

Further, applicant respectfully disagrees with the examiner's statement that the anti-reflective layer 215 is optional. All of the drawings include the anti-reflective layer 215 and the specification does not describe the anti-reflective layer 215 as optional. Additionally, Brennan fails to disclose either inherently or expressly metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer. Instead, Brennan relies on the sidewalls extending beyond the height of the interconnect to act as a guide for the via etching process. (Brennan, FIGs. 2G and 2H).

As Brennan fails to expressly or inherently teach every element of claim 1 as amended, applicant submits that claim 1 is not anticipated by Brennan. As such, claim 1 is allowable.

Claims 2 through 15 and 100 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 5 is further allowable as Brennan fails to inherently or expressly disclose a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

Claim 12 is further allowable as Brennan fails to inherently or expressly disclose a dielectric layer on the conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

a single conducting layer as recited in claim 1 because Liu would include a conducting layer 6 and the metal barrier layer 8.

Further, applicant submits that Liu teaches the metal barrier layer 8 comprises materials such as TaN, TiN or Ta which are not conducting metals. (Liu, col. 3, lines 39-41). Thus, metal barrier layer 8 is not a conducting layer. As the upper surface of the conducting layer 6 is in contact with the metal barrier layer 8, Liu does not inherently or expressly disclose "said single conducting layer including an upper surface out of contact with any metal" as recited in claim 1. Accordingly, Liu fails to expressly or inherently teach every element of claim 1. As such, claim 1 is allowable.

Claims 2 through 15 and 100 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 12 is further allowable as Liu fails to expressly or inherently teach a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

Claim 13 is further allowable as Liu fails to expressly or inherently teach that the dielectric layer comprises a low dielectric constant material.

Anticipation Rejection Based on U.S. Patent 6,242,340 B1 to Lee

Claims 16, 19, 20, 101, 116, 119, 120, and 129 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lee (U.S. Patent 6,242,340 B1). Applicant respectfully traverses this rejection, as hereinafter set forth.

Lee discloses a method of forming an interconnect layer wherein the interconnect layer comprises a substrate 20 having a dielectric layer 22 thereon. The dielectric layer 22 includes a trench filled with a conducting metal (first interconnect) 28. An insulation layer 30 overlays the first interconnect 28 and underlies a second dielectric layer 32. A second trench is formed in the second dielectric layer 32. The trench includes spacers 36a that extend to insulating layer 30 and is filled with a second conducting metal. 40. (Lee, FIGs. 3A-3F and col. 3-4, lines 60-67).

By way of contrast, independent claims 16 and 116 of the presently claimed invention each include the similar element of “a metal spacer abutting at least one sidewall of said aperture defining said conductive line, said metal spacer in contact with said underlying metal layer”. Applicant respectfully submits that Lee does not inherently or expressly teach this element. Instead, Lee discloses a substrate 20 including a first interconnect 28 in contact with a second interconnect 40. Spacers 36a on the side of the second interconnect 40 only extend to a second insulating layer 30 and do not contact the underlying first interconnect 28. Further, applicant respectfully submits that Lee teaches away from excluding the second insulating layer 30 as Lee teaches the second insulating layer 30 functions as an etch stop. (Lee, col. 4, lines 39-40). As Lee fails to inherently or expressly teach every element of independent claims 16 and 116 of the presently claimed invention, applicant respectfully submits that Lee does not anticipate these claims.

Claims 17 through 28 and 101 are each allowable as depending, either directly or indirectly, from allowable claim 16.

Claims 117 through 129 are each allowable as depending, either directly or indirectly, from allowable claim 116.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent 6,074,943 to Brennan et al. in view of U.S. Patent 6,166,439 to Cox

Claims 2, 3, 9, 100, 102 through 113, and 115 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brennan et al. (U.S. Patent 6,074,943) in view of Cox (U.S. Patent 6,166,439). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or

suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The discussion of Brennan, above, is incorporated herein by reference. Cox discloses a low dielectric constant material and method of application to isolate conductive lines. Cox discloses a semiconductor device which includes a substrate and a conductive pattern formed on the substrate. The conductive pattern includes at least two conductive lines adjacent one another. A low dielectric constant material is disposed between the at least two conductive lines.

With respect to claims 2, 3, 9, and 100, the Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of claim 1 as proposed to be amended, the prior art referenced as rendering dependent claims 2, 3, 9 and 100 obvious, cannot serve as a basis for rejection.

By way of contrast with the proposed combination of references, claim 102 as amended recites a structure for transmitting a signal across a semiconductor device, said structure comprising a substrate comprising a substantially planar upper surface; and a conductive line extending over said upper surface and isolated therefrom by a dielectric layer at least underlying said conductive line, said conductive line comprising: a metal layer above said dielectric layer, said metal layer defining a pattern on a portion of the substrate upper surface; a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls, wherein an upper surface of said single conductive layer is out of contact with any metal; and metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer.

Applicant respectfully submits that Brennan and Cox fail to teach or suggest metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer. Instead, Brennan relies on the sidewalls extending beyond the height of the interconnect to

act as a guide for the via etching process. (Brennan, FIGs. 2G and 2H). Cox lacks any disclosure of sidewalls.

As the proposed combination of Brennan and Cox fail to teach or suggest every element of claim 102, the claim is not rendered obvious in view of the proposed combination. Thus, claim 102 is allowable.

Claims 103 through 115 are each allowable as depending, either directly or indirectly, from allowable claim 102.

Claim 109 is further allowable as the proposed combination fails to teach or suggest the single conducting layer is an aluminum-copper alloy.

Claim 112 is further allowable as the proposed combination fails to teach or suggest a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

Claim 114 is further allowable as the proposed combination fails to teach or suggest the dielectric layer is fluorine-doped silicon oxide.

Obviousness Rejection Based on U.S. Patent 6,074,943 to Brennan et al. in view of U.S. Patent 6,046,502 to Matsuno

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Brennan et al. (U.S. Patent 6,074,943) in view of Matsuno (U.S. Patent 6,046,502). Applicant respectfully traverses this rejection, as hereinafter set forth.

Brennan is discussed above and incorporated herein. Matsuno is directed toward a semiconductor device with improved adhesion between a titanium-based metal layer and an insulation film and fails to cure the deficiencies of Brennan. Further, the Court of Appeals for the Federal Circuit has stated that “dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.” *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every

limitation of claim 1, the prior art referenced as rendering dependent claim 14 obvious cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent 6,242,340 B1 to Lee in view of U.S. Patent 6,197,682 B1 to Drynan et al.

Claims 17, 18, 23 through 28, 117, 188, and 123 through 128 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee (U.S. Patent 6,242,340 B1) in view of Drynan et al. (U.S. Patent 6,197,682 B1). Applicant respectfully traverses this rejection, as hereinafter set forth.

The discussion of Lee is incorporated herein. Drynan teaches a structure of a contact hole in a semiconductor device and method of manufacturing the same. The structure includes a substrate 101 with an overlying silicon dioxide dielectric film 102, an overlying silicon nitride layer 103, a first wiring layer 108ac surrounded by a first dielectric layer 112, silicon nitride spacers 116a defining a contact plug 117 within the first dielectric layer 112, a overlying silicon nitride layer 113, a second wiring layer 118ac surrounded by a second dielectric layer 122, an overlying silicon nitride layer 123 and spacers 136a adjacent a conductive film 125. A second contact plug 137 fills in the space defined by spacers 136a.

The Court of Appeals for the Federal Circuit has stated that “dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.” In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of claims 16 and 116, the art referenced as rendering dependent claims 17, 18, 23 through 28, 117, 118, and 123 through 128 obvious cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent 6,242,340 B1 to Lee in view of U.S. Patent 6,166,439 to Cox

remain which might be resolved by a telephone conference, he is respectfully invited to contact applicant's undersigned attorney.

Respectfully Submitted,


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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended three times) A metallization structure for a semiconductor device, comprising:
a substrate comprising a substantially planar upper surface; and
a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising:
a metal layer defining a pattern on a portion of the substrate upper surface;
a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls and said single conducting layer including an upper surface out of contact with any metal; and
metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer.

16. (Amended three times) A metallization structure for a semiconductor device, comprising:
a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate;
a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture defining said conductive line;
a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture, said metal spacer in contact with said underlying metal layer; and
a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.

102. (Amended twice) A structure for transmitting a signal across a semiconductor device, said structure comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line extending over said upper surface and isolated therefrom by a dielectric layer at least underlying said conductive line, said conductive line comprising:

a metal layer above said dielectric layer, said metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls, wherein an upper surface of said single conductive layer is out of contact with any metal; and

metal spacers flanking and substantially the same height as the sidewalls of the single conducting layer and metal layer

116. (Amended twice) A structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising:

a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line;

a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture, said metal spacer in contact with said underlying metal layer; and

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture.